


Revision : 1.12

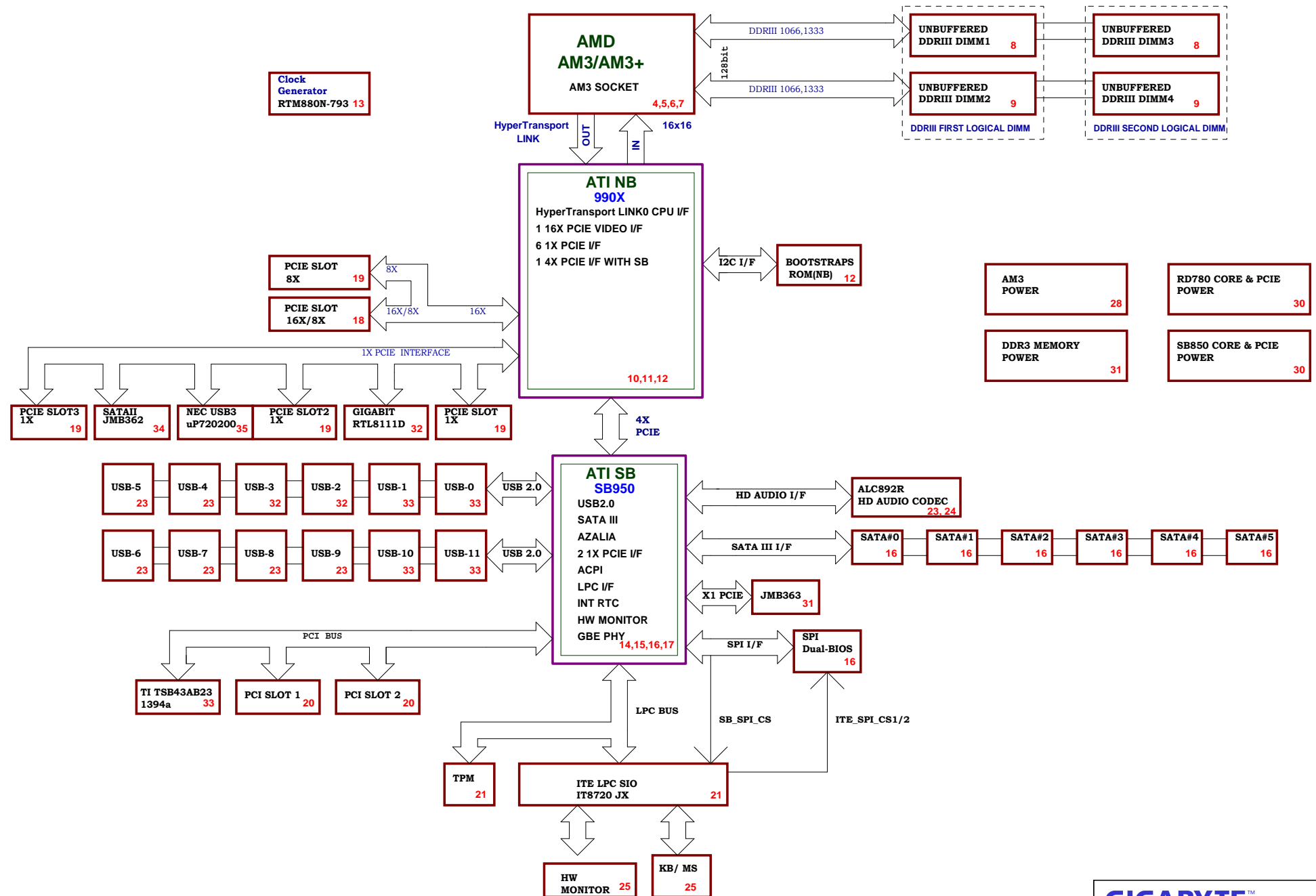
PAGE	TITLE
01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU HYPER TRANSPORT
05	CPU DDRIII MEMORY
06	CPU CONTROL
07	CPU POWER & GND
08	DDRIII CHANNEL A
09	DDRIII CHANNEL B
10	RD980 HT-LINK I/F
11	RD980 PCIE I/F ,SWITCH
12	RD980 SYSTEM I/F
13	RD980 STRAPS ,SPMEM, POWER, GND
14	9LPR477D
15	SB950 PCIE/PCI/CPU/LPC
16	SB950 ACPI/USB/GPIO/AUDIO
17	SB950 SATA/SPI/IDE/HWM
18	SB950 POWER & GND
19	PCI EXPRESS x16
20	PCI_E x8 ,PCI_E x1 SLOT 1,2
21	PCI SLOT 1, 2
22	IT8720 JX LPC IO ,Dual-BIOS ,TPM
23	ALC889R CODEC
24	AUDIO JACK
25	FAN/HWMO/COM/ KB_MS

[illegible]

P-Code: U98094-0

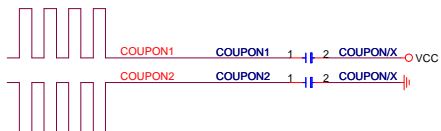
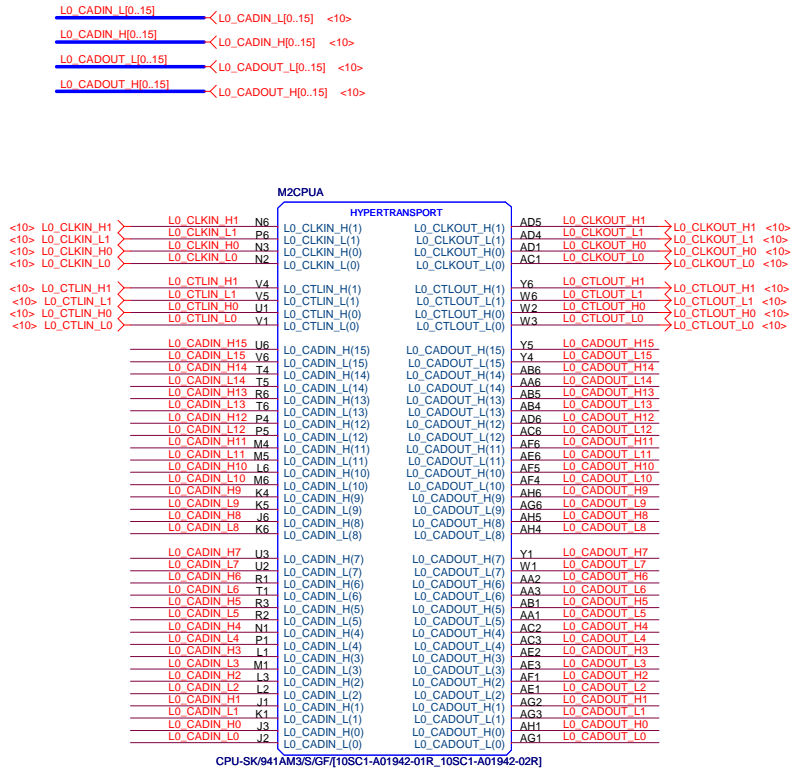
[illegible][illegible]

			
Title			
BOM & PCB HISTORY			
Size	Document Number		Rev
Custom	GA-990XA-UD3		1.12
Date:	Thursday, May 03, 2012	Sheet	2 of 35

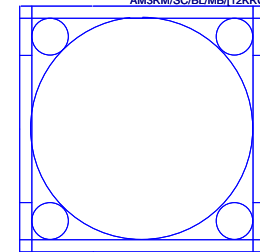


CPU_VDD_RUN = VCORE
 CPU_VDDA_RUN = VDDA25
 VLDT_RUN = VCC12_HT
 CPU_VDDIO_SUS = DDR15V
 CPU_VDDR = CPU_VDDR12

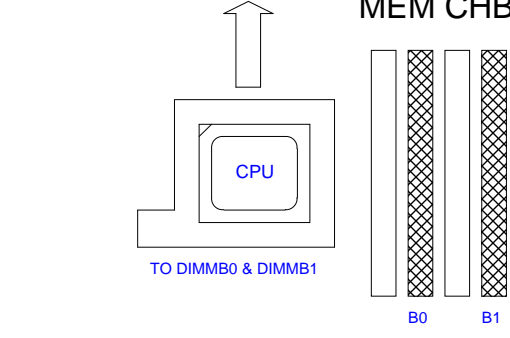
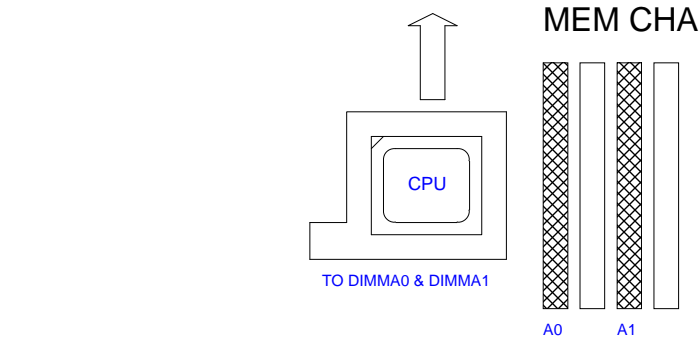
VLDT_A = VCC12_HT
 VLDT_B = HT12B

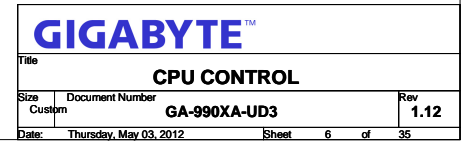


M2CPU
 AM3RM/SC/BL/MB/12KRC-04K812-31R

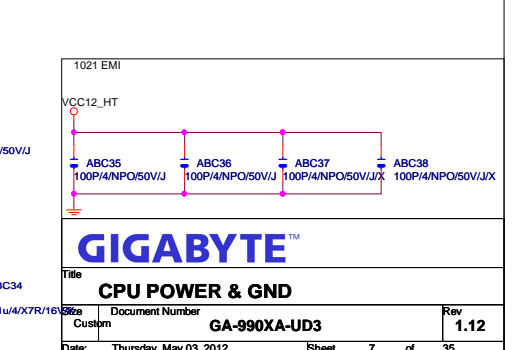
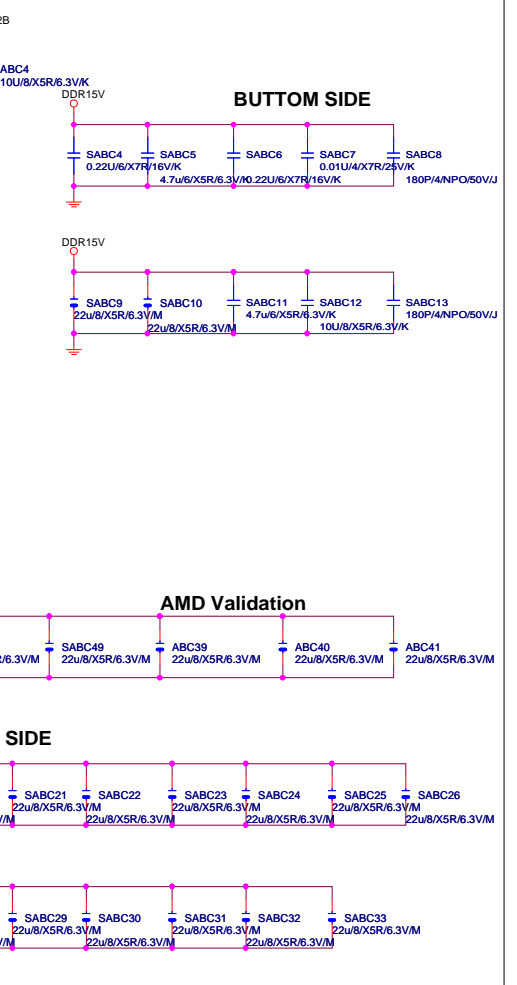


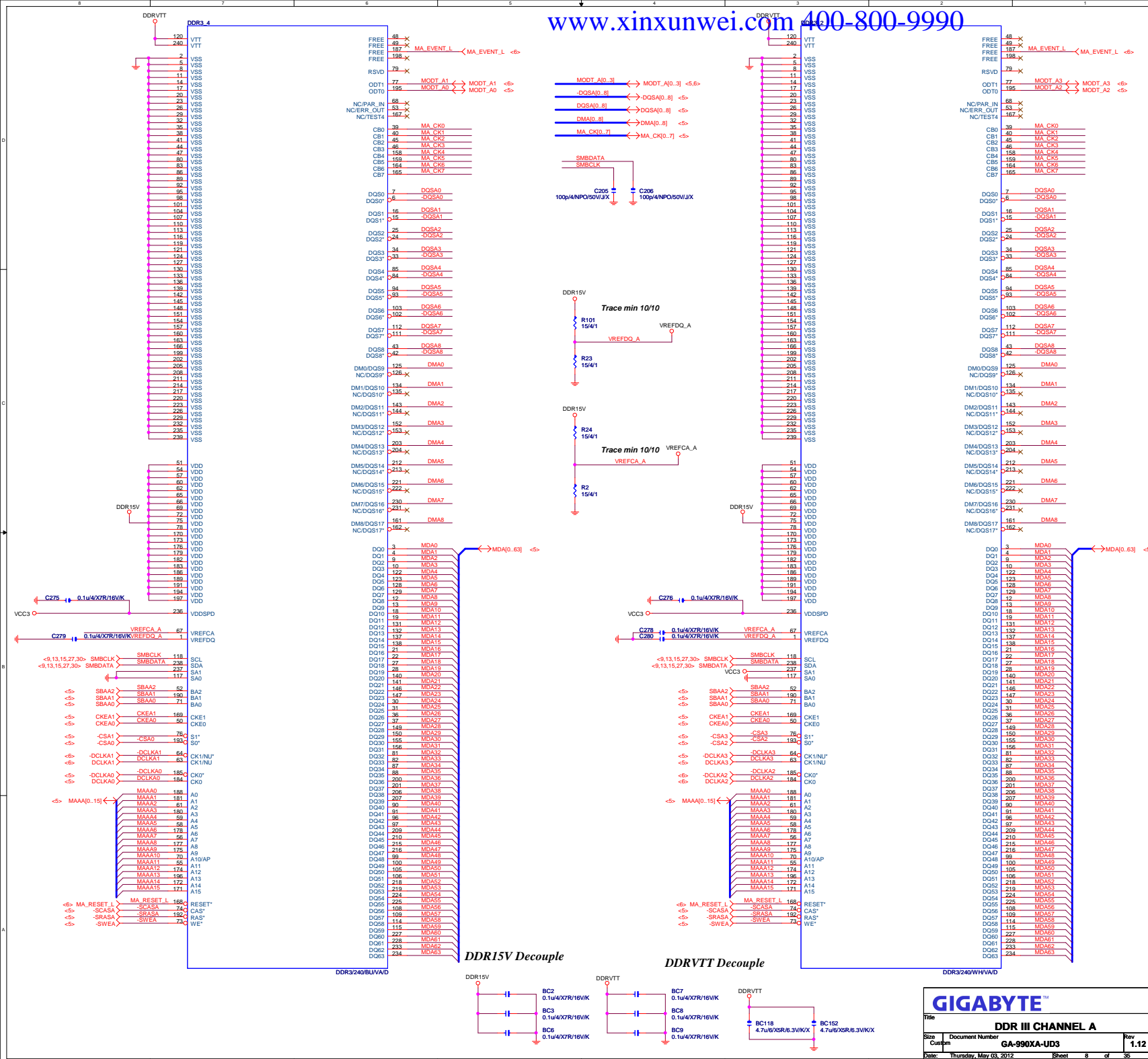
GIGABYTE™			
Title			
CPU HYPER TRANSPORT			
Size	Document Number	Rev	
Custom	GA-990XA-UD3	1.12	
Date:	Thursday, May 03, 2012	Sheet	4 of 35

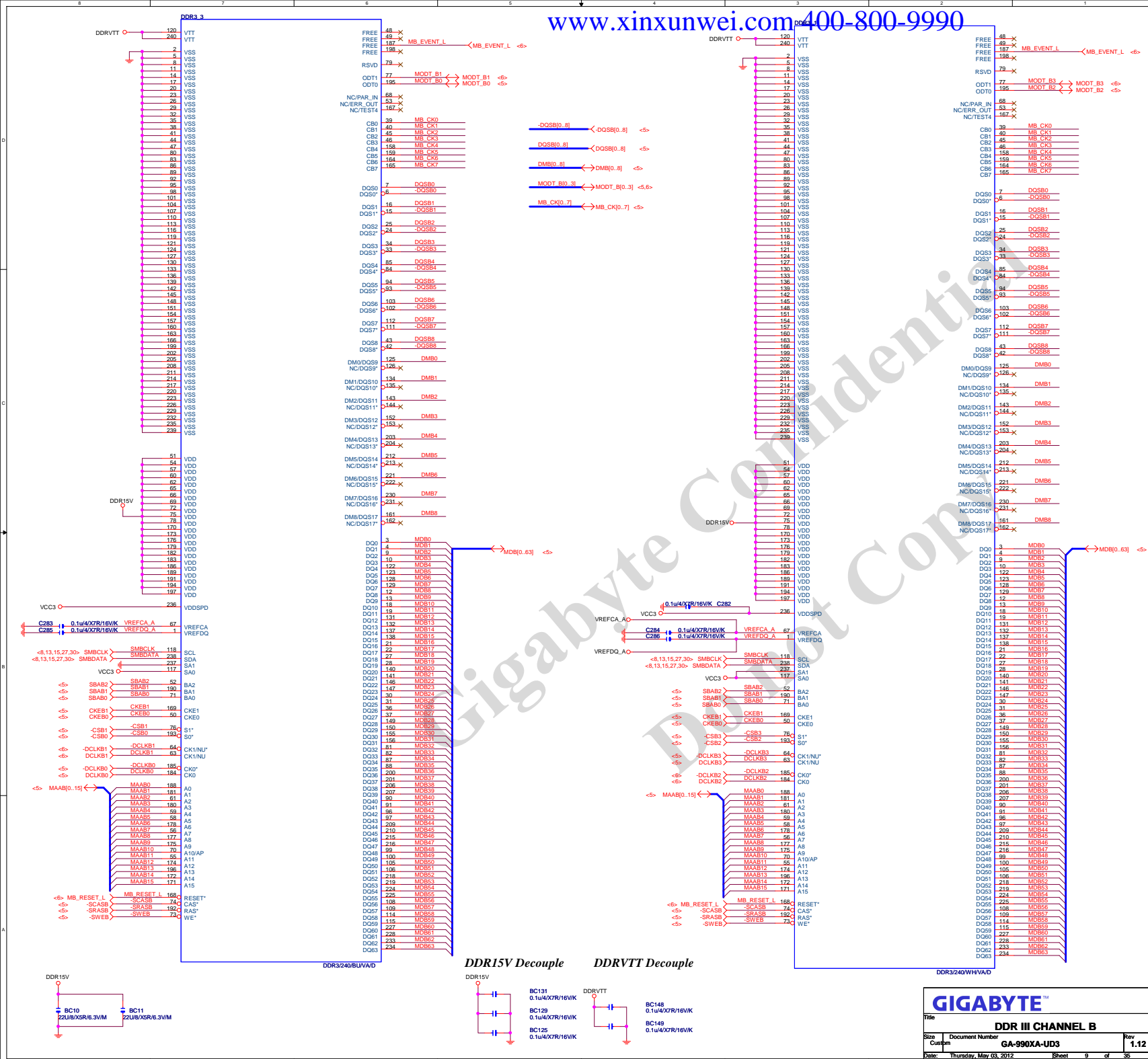


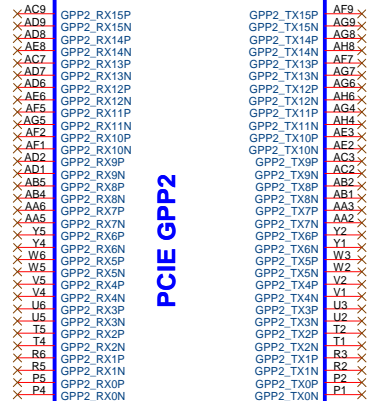
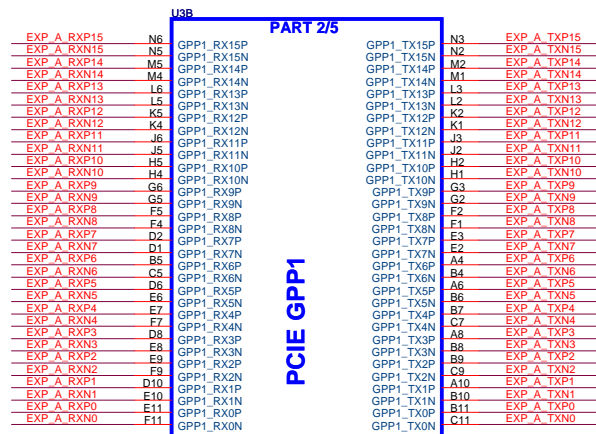


GIGABYTE™			
Title			
CPU CONTROL			
Size	Document Number	Rev	
Custom	GA-990XA-UD3	1.12	
Date:	Thursday, May 03, 2012	Sheet	6 of 35

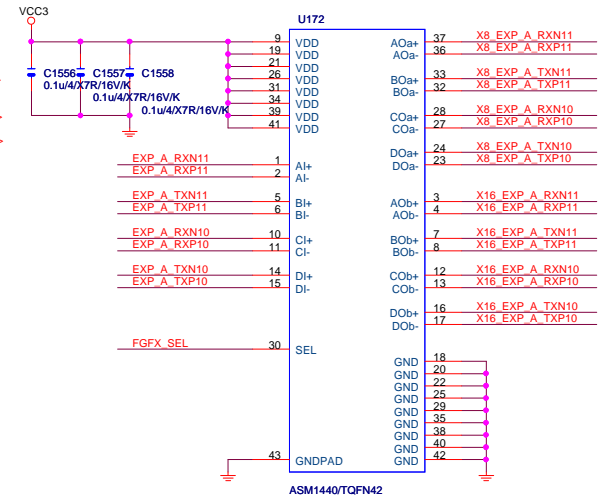
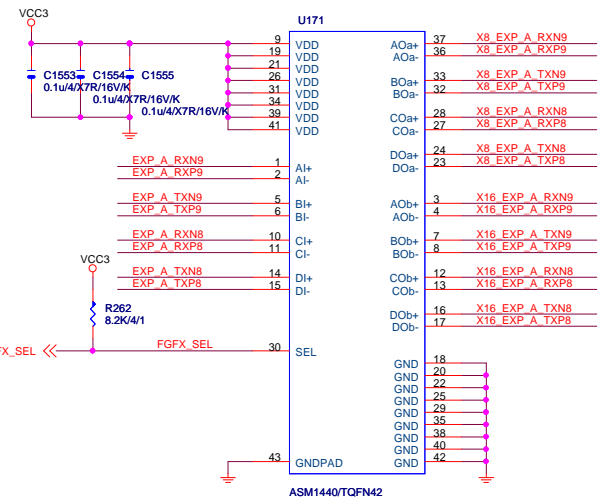
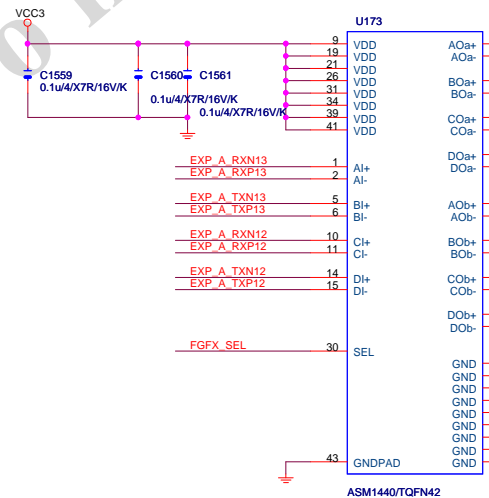
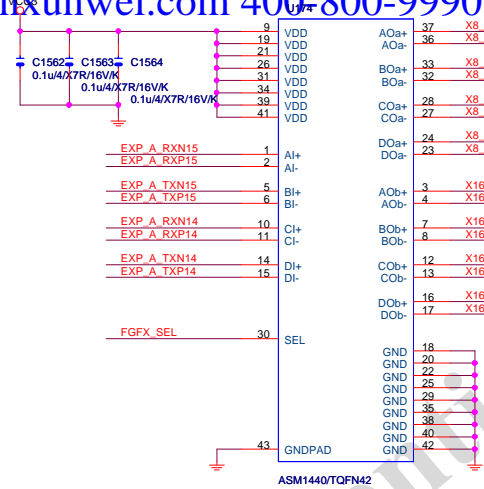








RD980/BGA692



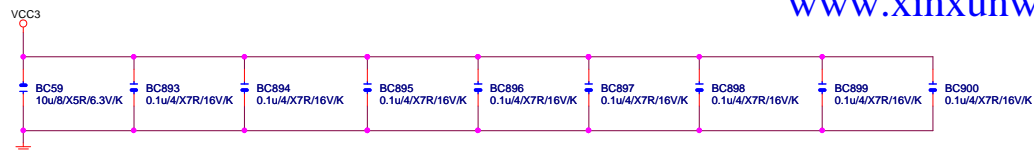
Function	SEL
xI--> x0a	L (X8)
xI--> x0b	H (X16)



Title	RD990 PCIE I/F ,Switch
-------	-------------------------------

Size	Document Number	Rev
Custom	GA-990XA-UD3	1.12

Date: Thursday, May 03, 2012 Sheet 11 of 35



- 1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO U800 AS POSSIBLE
- 2- ROUTE ALL SRCCLKTx AND SRCCLKCx AS DIFFERENT PAIR RULE
- 3- PUT DECOUPLING CAPS CLOSE TO U800 POWER PIN

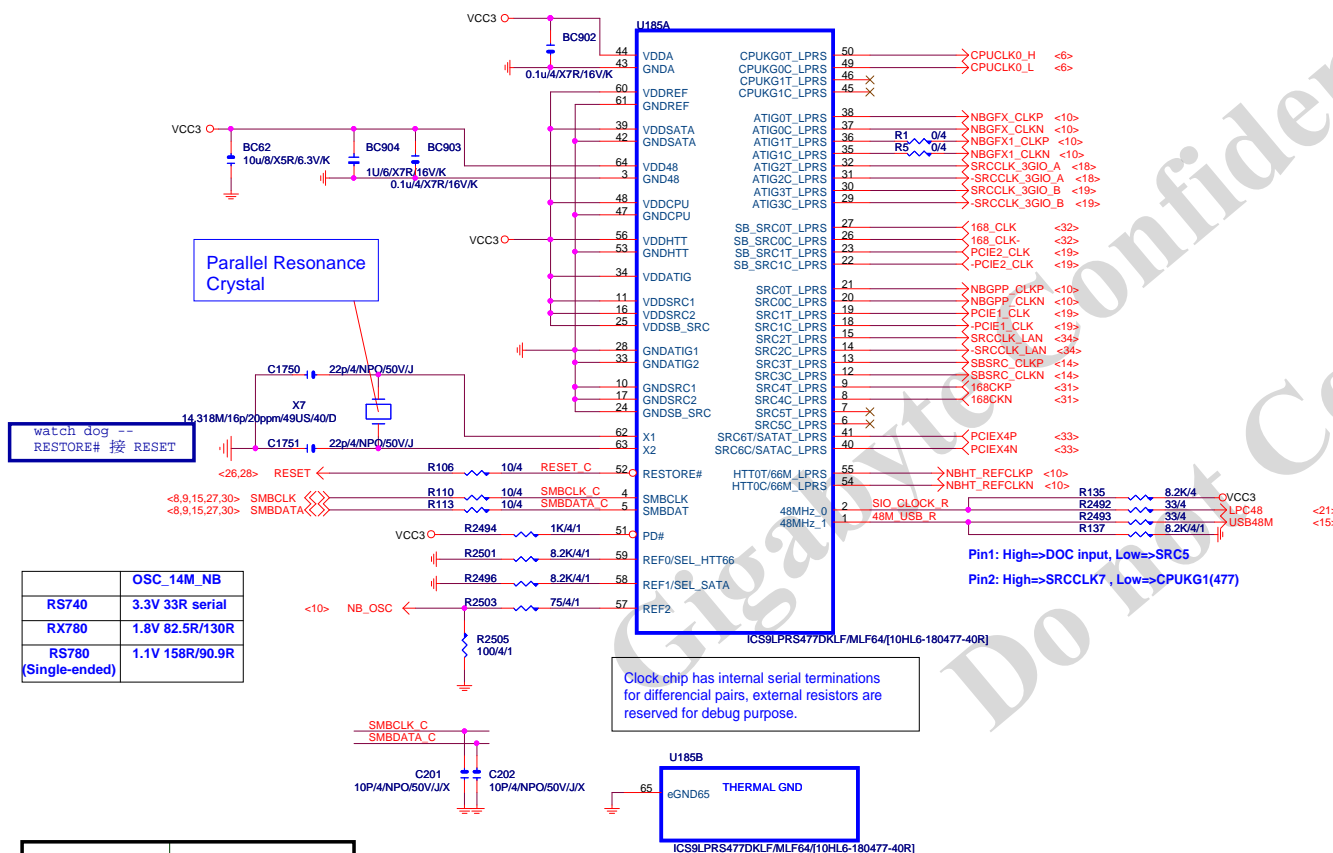


Place R800/801 less than 500 mils away from U800
R851 less than 100 mils away from R800/801
route CPU clock as 100ohm differential pair

NB CLOCK INPUT TABLE

NB CLOCKS		RS740	RX780	RS780	
HT_REFCLKP	66M SE(SE)			100M DIFF	
HT_REFCLKN	NC		100M DIFF	100M DIFF	
REFCLK_P	14M SE (3.3V)		14M SE (1.8V)	14M SE (1.1V)	100M DIFF
REFCLK_N	NC	NC		vref	100M DIFF
GFX_REFCLK*	100M DIFF	100M DIFF		100M DIFF	
GPP_REFCLK	NC	100M DIFF		100M DIFF(OUT)	
GPSPB_REFCLK	100M DIFF	100M DIFF		100M DIFF	

* the GFX_REFCLK input is required for all cases



	OSC_14M_NB
RS740	3.3V 33R serial
RX780	1.8V 82.5R/130R
RS780 (Single-ended)	1.1V 158R/90.9R

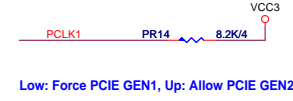
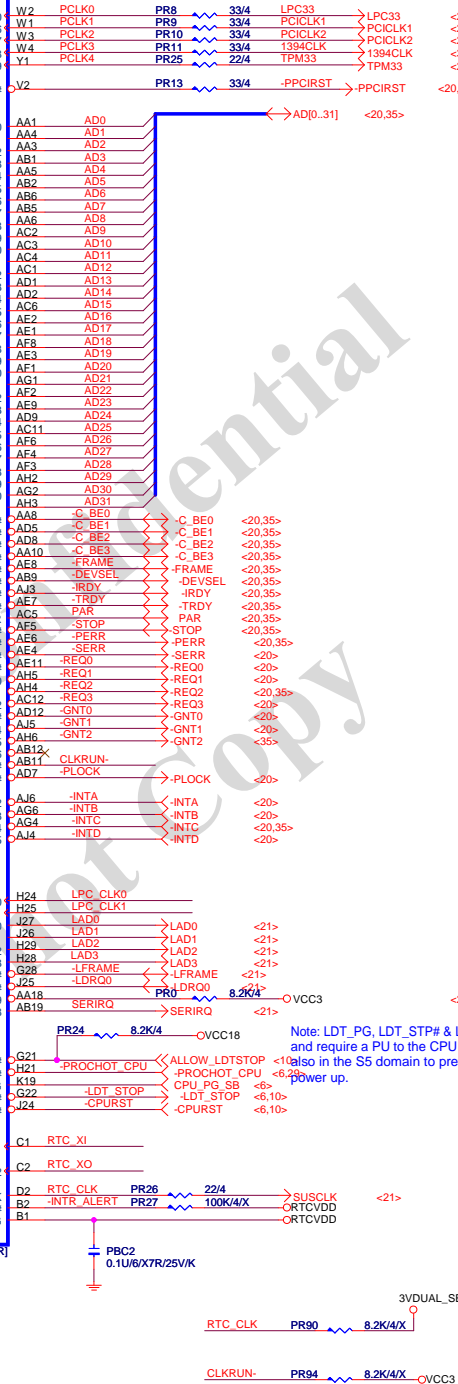
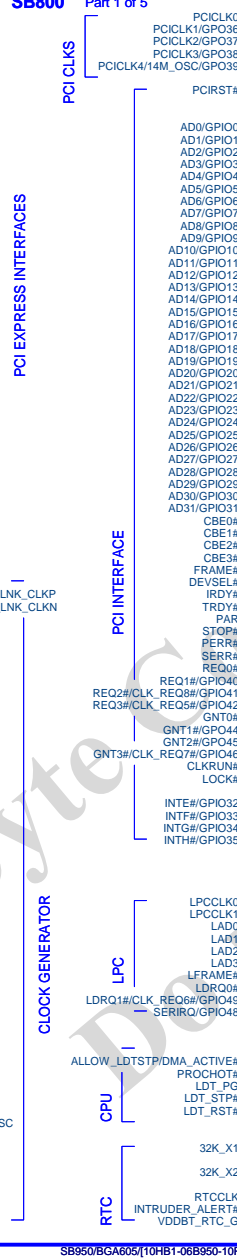
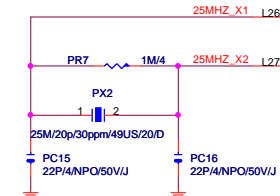
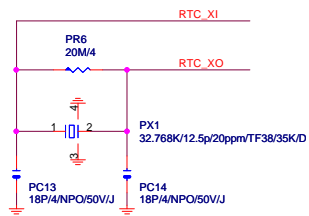
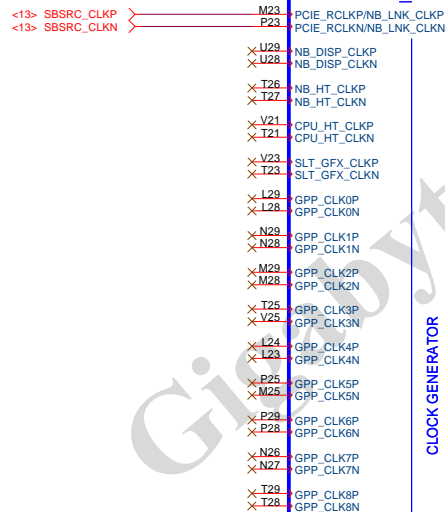
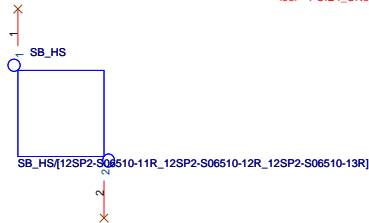
REF0/SEL_HTT66	HTT CLOCK
0	100.00 DIFFERENTIAL
1	66.66 SINGLE END

REF1/SEL_SATA	SRC6/SATA
0	100.00 DIFFERENTIAL SPREADING SRC CLOCK
1	100.00 NON-SPREADING DIFFERENTIAL SATA CLOCK

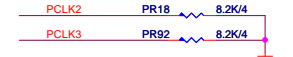
				
Title				
RTM880N-793				
Size	Document Number			Rev
Custom	GA-990XA-UD3			1.12
Date:	Thursday, May 03, 2012	Sheet	13	of 35

PLACE THESE PCIE AC COUPLING
CAPS CLOSE TO SB850

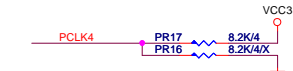
S.B HEATSINK



Low: Force PCIE GEN1, Up: Allow PCIE GEN2



	PCLK2	PCLK3
PULL HIGH	WATCHDOG TIMER ON NB_PWRGD ENABLED	USE DEBUG STRAPS
PULL LOW	WATCHDOG TIMER ON NB_PWRGD DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT

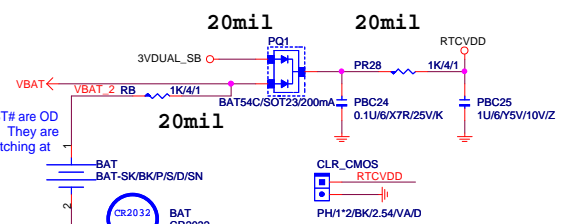


BIOS after boot setting
EC AOD-ACC



LPC_CLK0 LPC_CLK1

PULL HIGH	IMC ENABLED	CLKGEN ENABLED
PULL LOW	AOD Extreme IMC DISABLED	CLKGEN DISABLED
	DEFAULT	DEFAULT



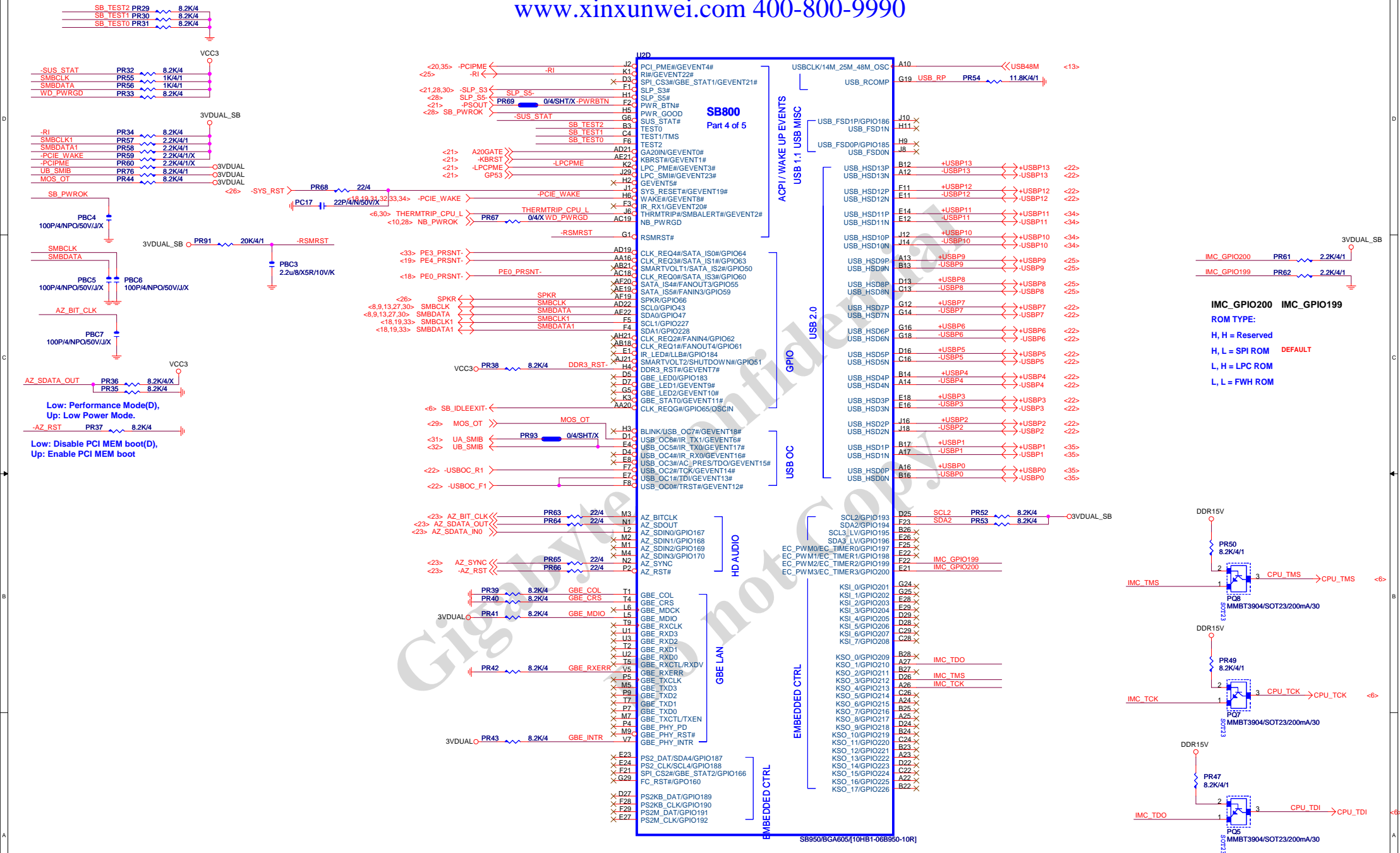
CLR_CMOS	
SHORT	CLEAR CMOS
OPEN	NORMAL

NOT ADD ICT FOR RTCVDD PIN

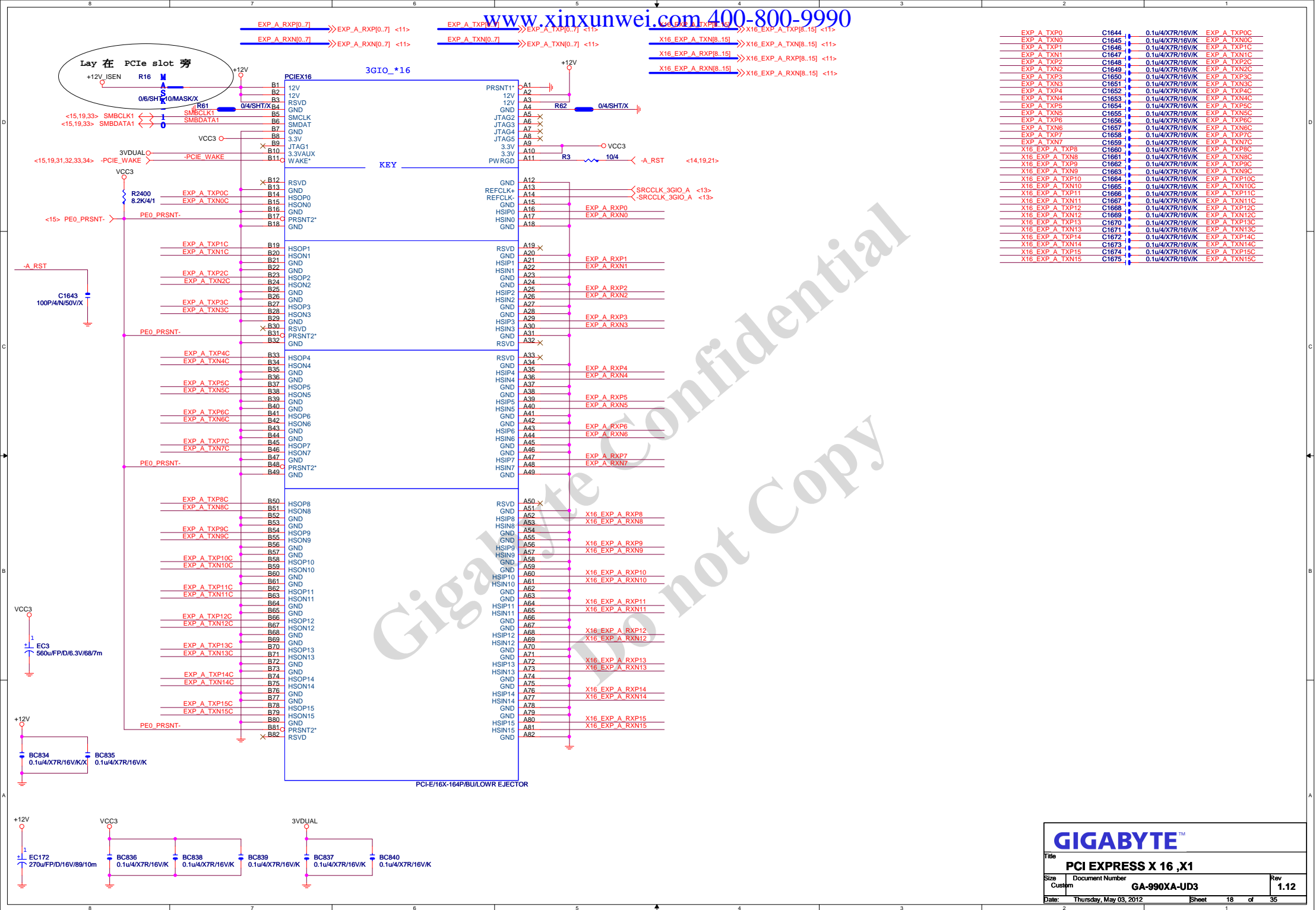
GIGABYTE™

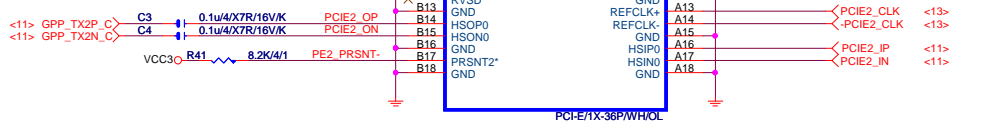
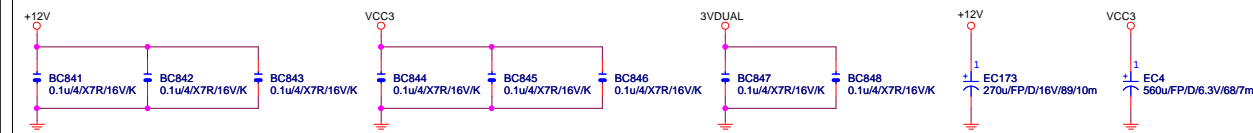
Title	ATI SB700 PCIE/PCI/CPU/LPC
-------	-----------------------------------

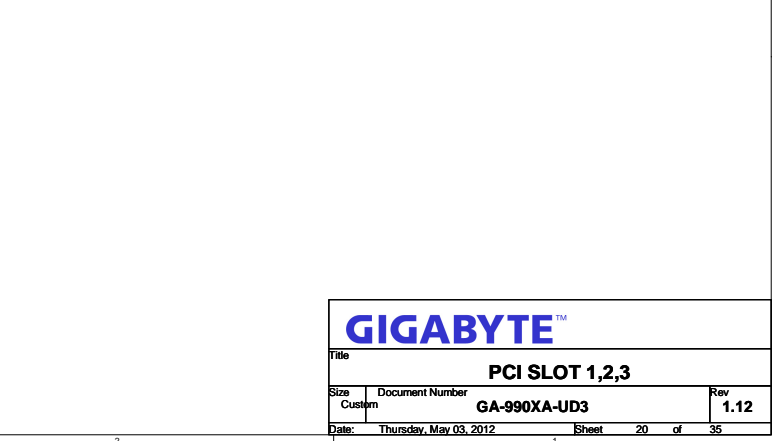
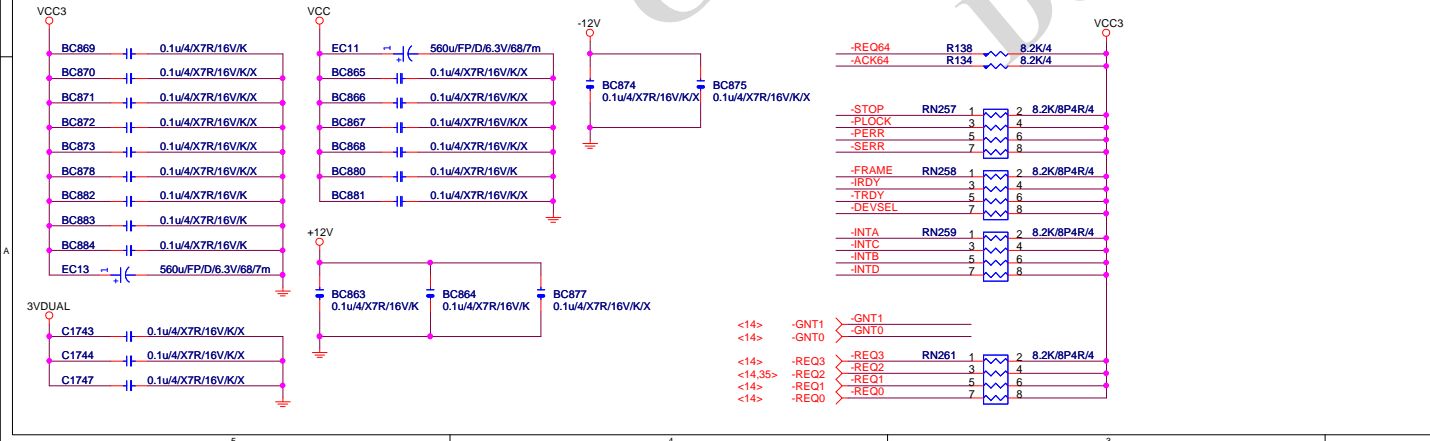
Size Custom	Document Number GA-990XA-UD3	Rev 1.12
Date: Thursday, May 03, 2012	Sheet 14 of 35	

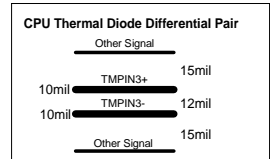





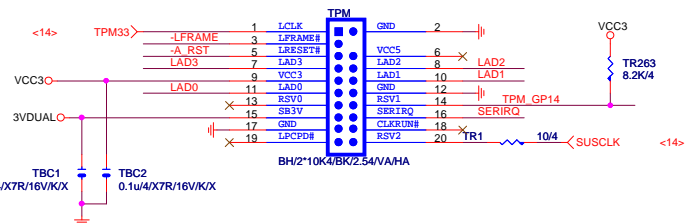
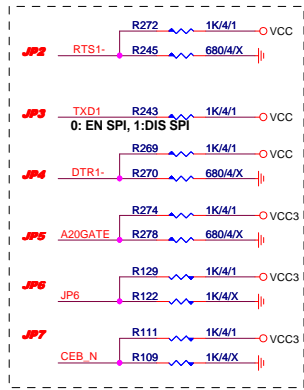


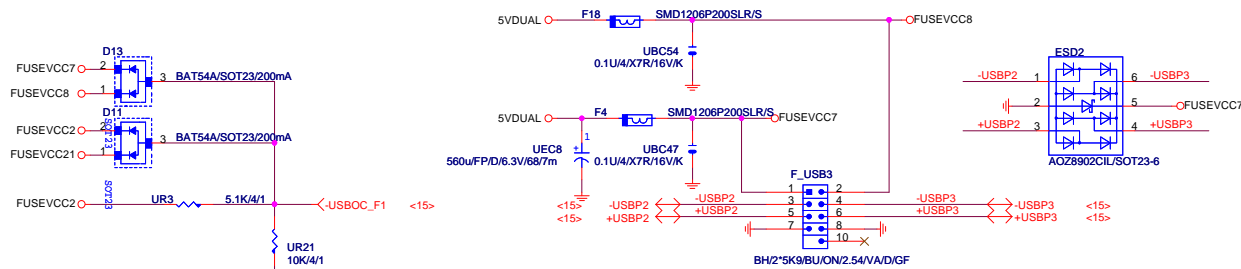




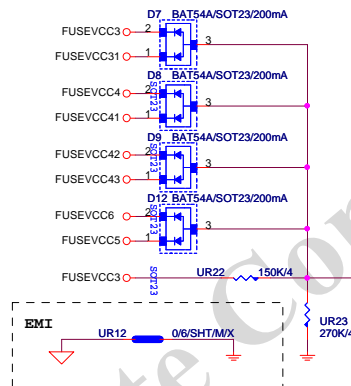
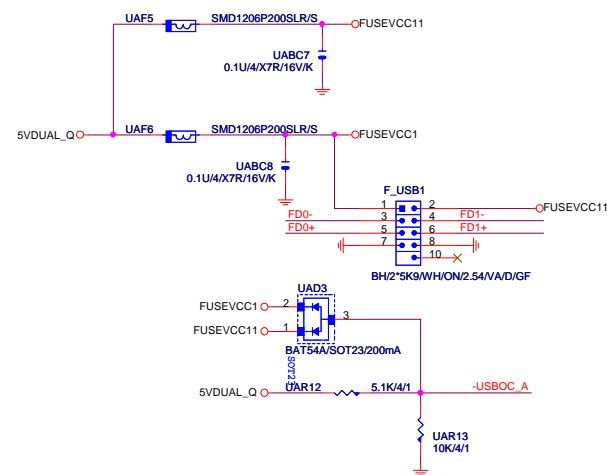


	Symbol	value	Description
JP1 Pin 69			
JP2 Pin 25	VIDO_EN	1	Disable VID output pins
		0	Enable VID output pins
JP3 Pin 27	Flashseg1_EN	1	Disabled.
		0	Flash I/F Address Segment 1 is enabled
JP4 Pin 29	K8PWR_EN	1	K8 power sequence disabled
		0	K8 power sequence enabled
JP3 & JP5 Pin 27 & Pin 77	FAN_CTL_SEL	11 Half Run	Default value of EC Index 15h/16h/17h is 40h
		10 No Run	Default value of EC Index 15h/16h/17h is 7Fh
		01 Full Run	Default value of EC Index 15h/16h/17h is 00h
		00 75% Run	Default value of EC Index 15h/16h/17h is 20h
JP5 Pin 77	WDT_EN	1	Disable WDT to rest PWROK
		0	Enable WDT to rest PWROK
JP6 Pin 60	SVID_EN	1	Disable SVID Function
		0	Enable SVID Function
JP7 Pin 97	Dual_BIOS_EN	1	Enable Dual BIOS Function for GigaByte Only
		0	Disable Dual BIOS Function for GigaByte Only

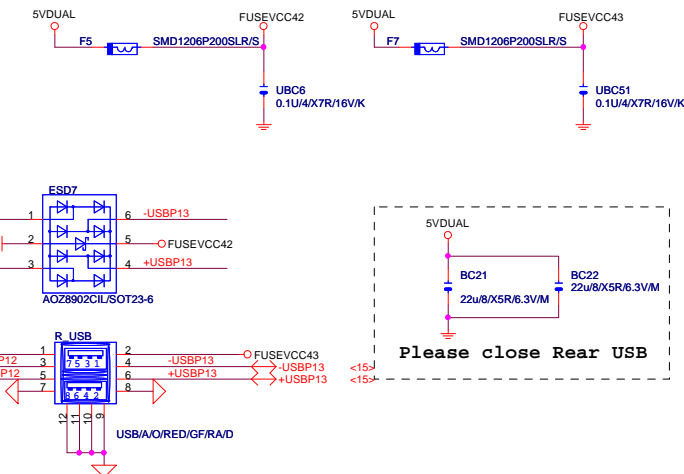




FRONT SIDE USB1

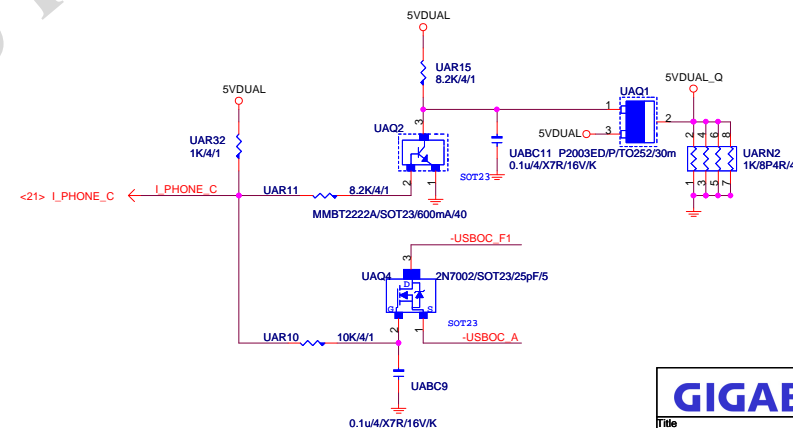
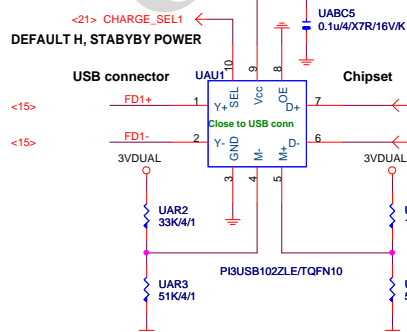
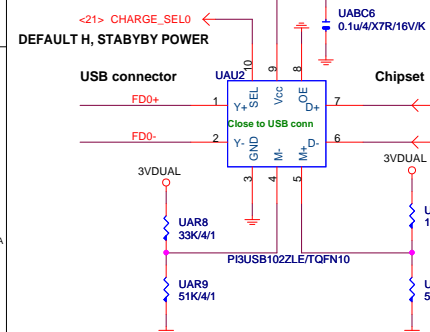


REAR USB



Please close Rear USB

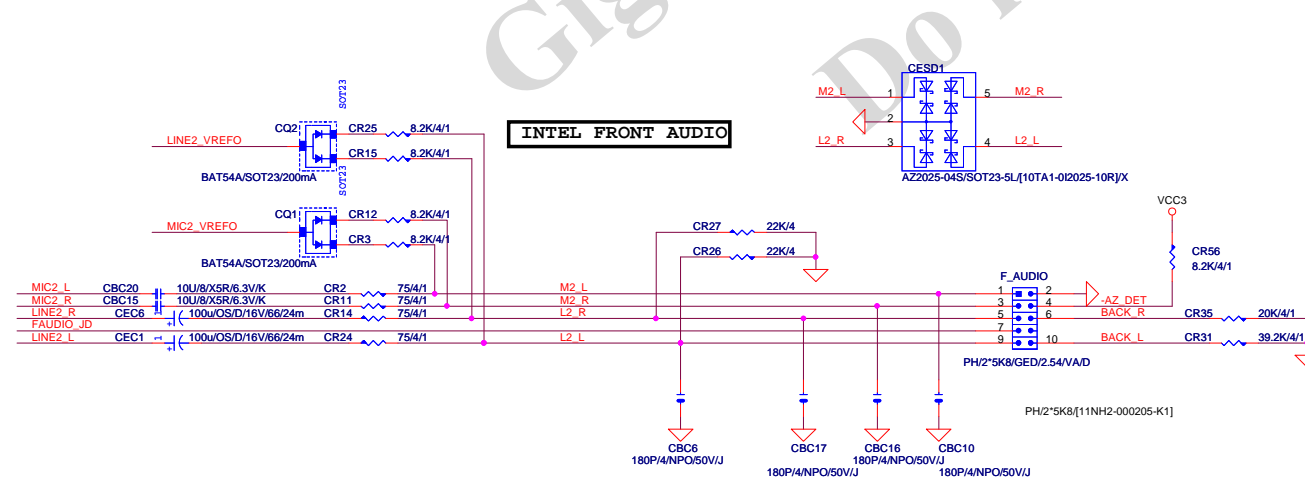
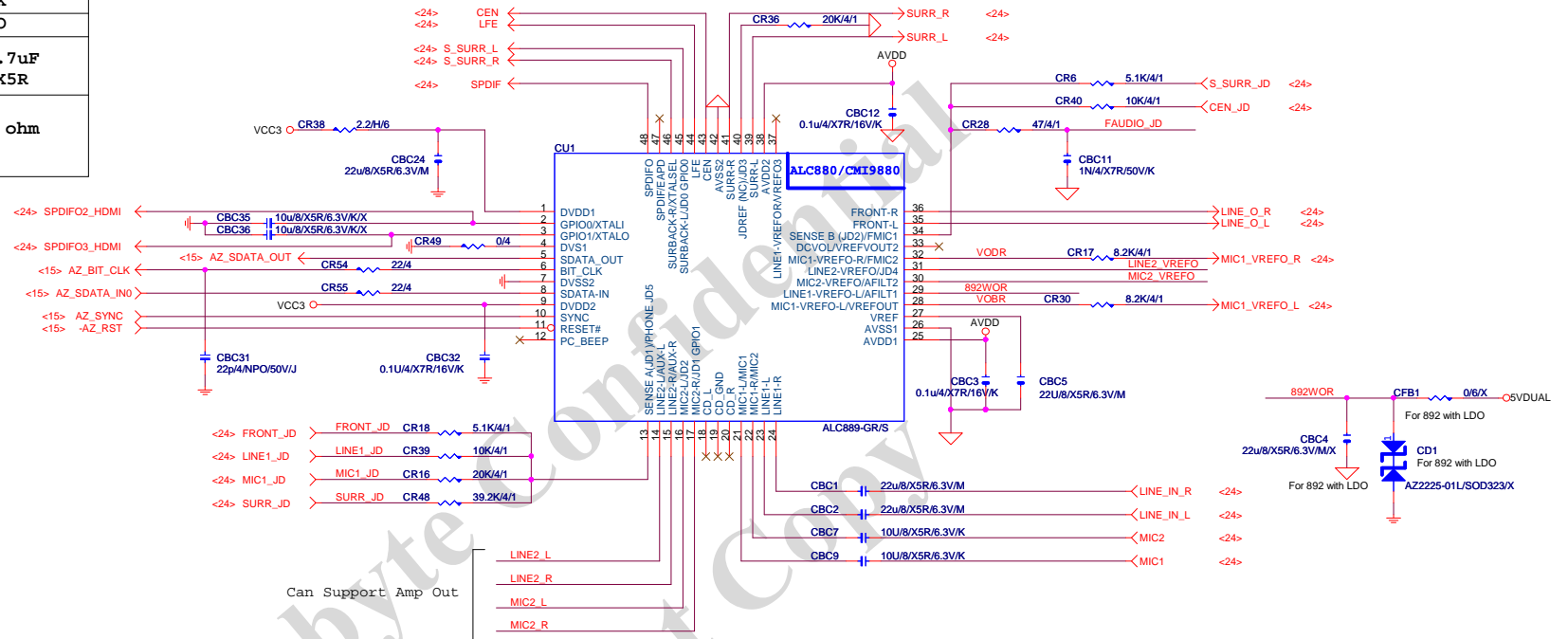
I_Phone charger circuit

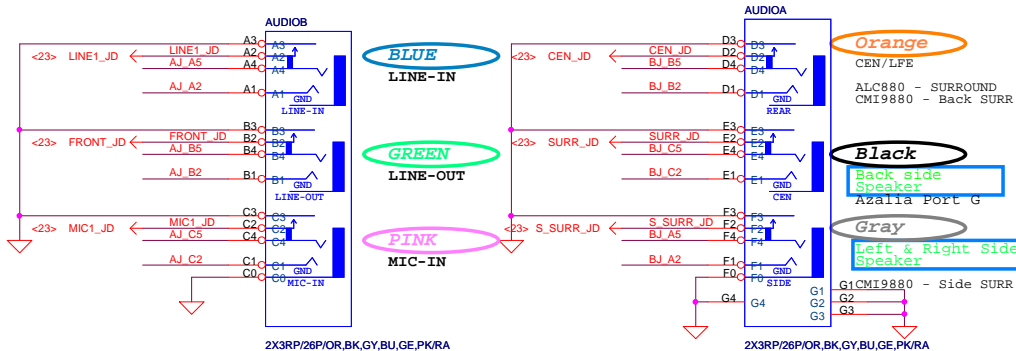
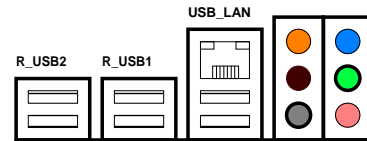
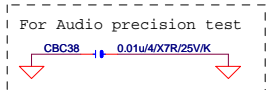
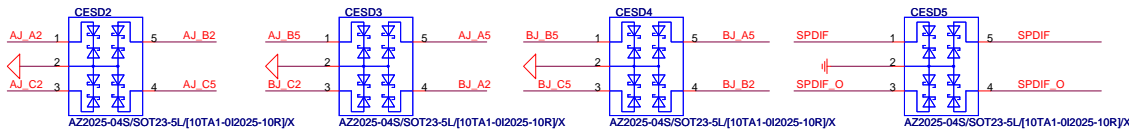
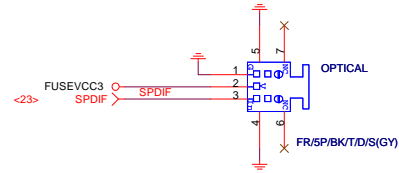
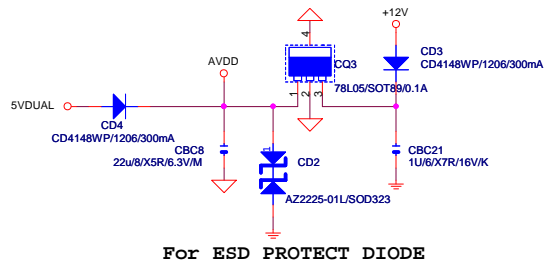
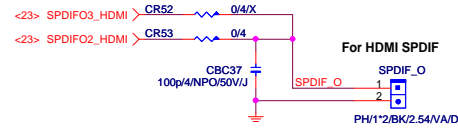
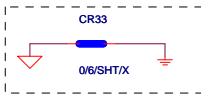


GIGABYTE™

Title		
COM/LPT/F_USB1_PWR		
Size	Document Number	Rev
Custom	GA-990XA-UD3	1.12
Date	Thursday, May 03, 2012	Sheet 22 of 35

	ALC892R	ALC889	ALC889A
CR16	X	X	O
CR24	X	X	O
CR25	X	O	O
CBC42	10uF/X5R	X	X
CR2	20K/1%	20K/1%	20K/0.1%
CR9	O	O	X
CR10	X	X	O
CBC10/CBC11/CBC12/ CBC13/CBC44/CBC45	4.7uF /X5R	10uF /X5R	4.7uF /X5R
CR4/CR8/CR18/CR23/ CR11/CR12/CR27/CR29/ CR49/CR50/CR43/CR44/ CR45/CR48/CR59/CR60	75 ohm	66 ohm or lower	75 ohm

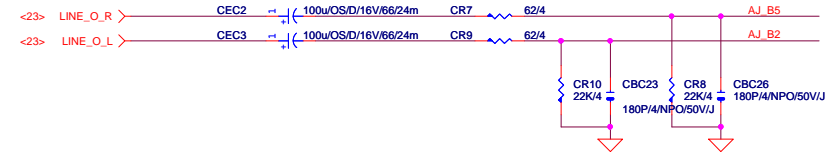




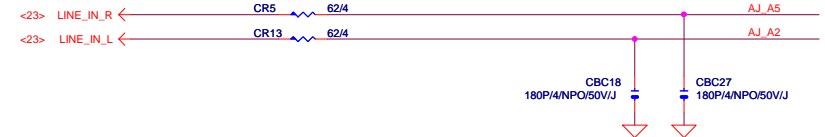
A3R7/13P/B/[11NR6-403006-01_11NR6-403006-02]
3R7+15P/[11NR6-403004-11]

A3R7/13P/0BG/[11NR6-403006-71]
3R7+15P/[11NR6-403004-31]

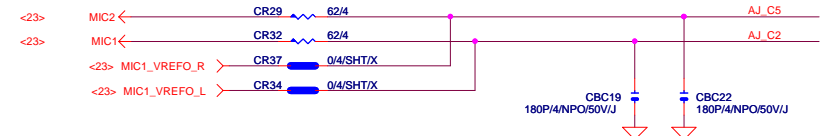
LINE OUT FRONT OUT



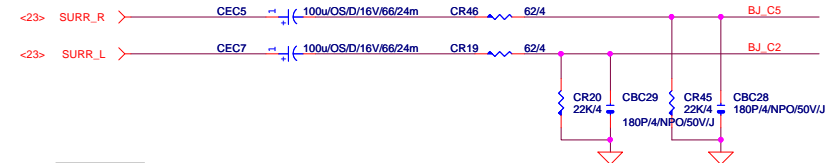
LINE-IN



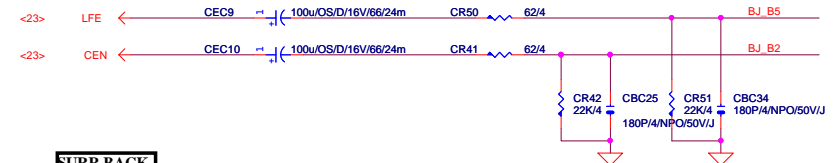
MIC



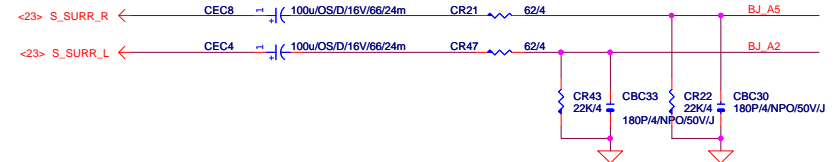
SURROUND



CEN/LFE



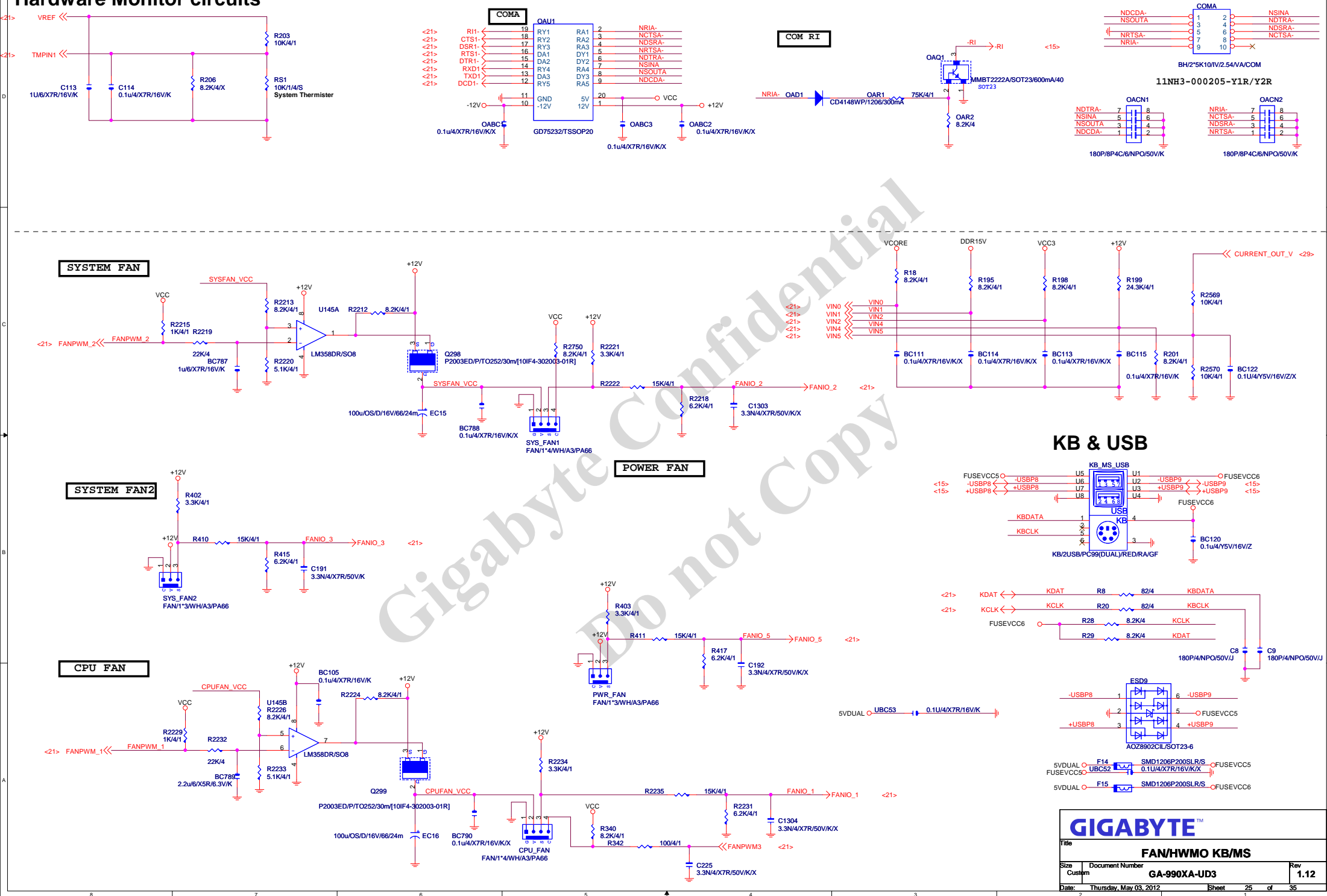
SURR BACK

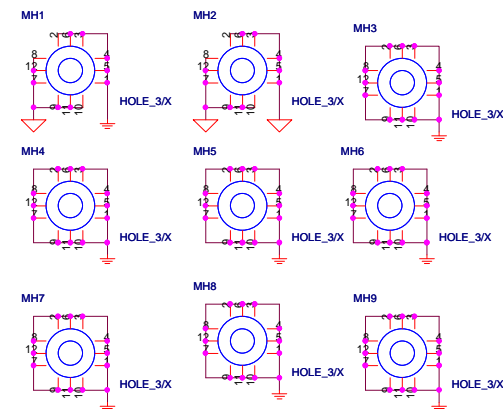
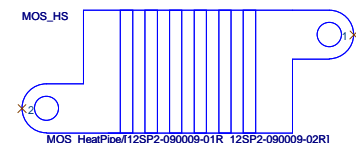
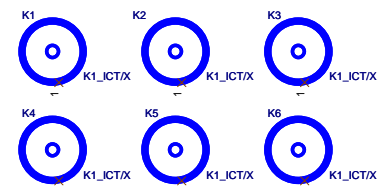
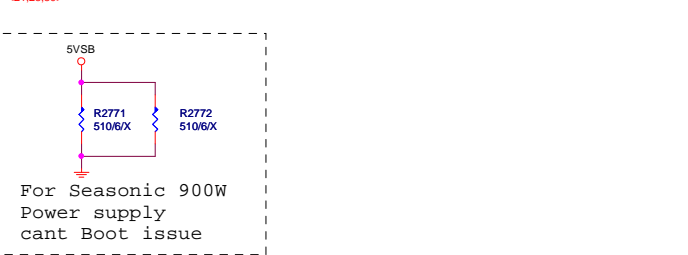
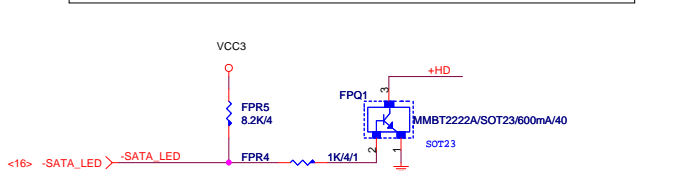
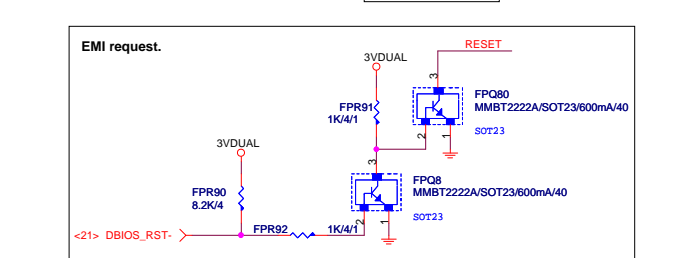
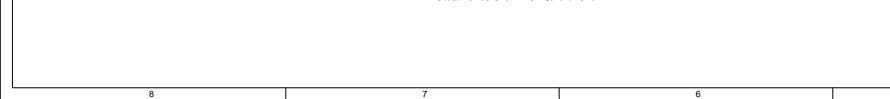
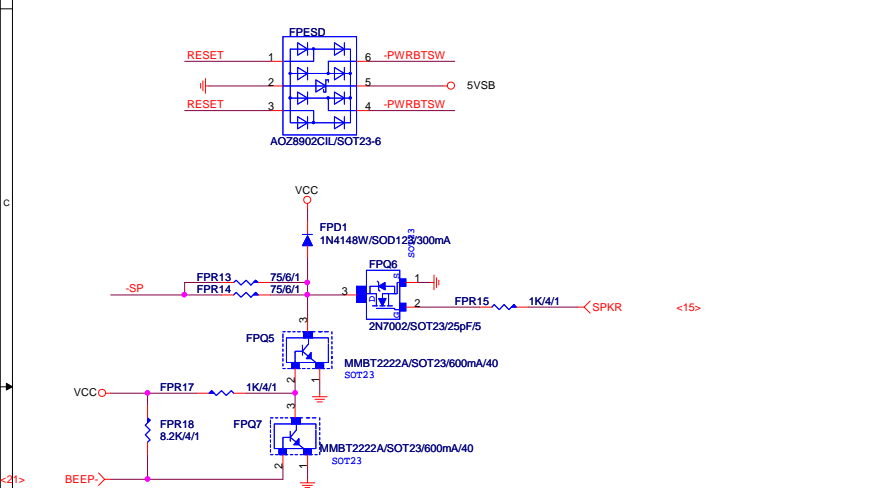


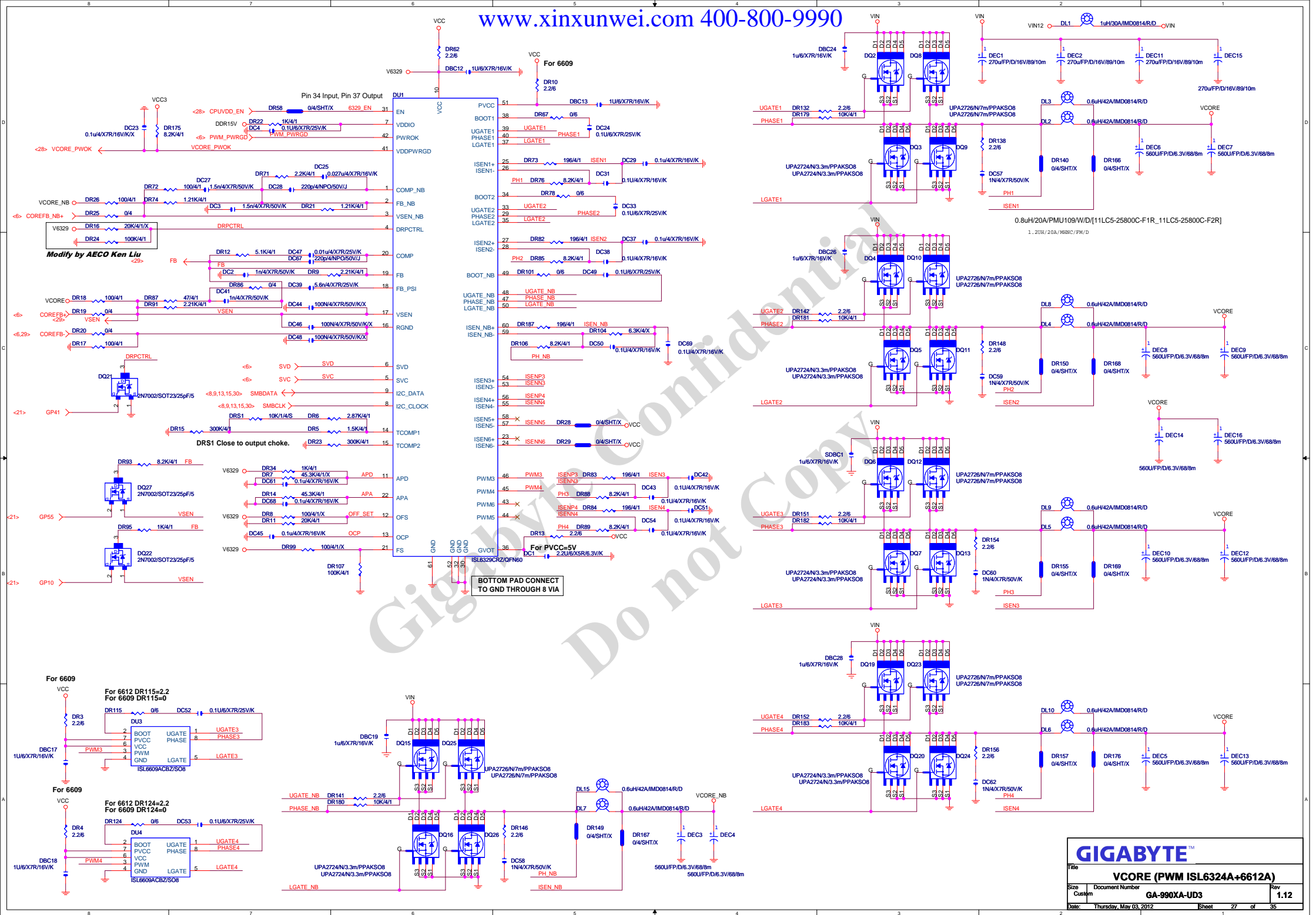
GIGABYTE

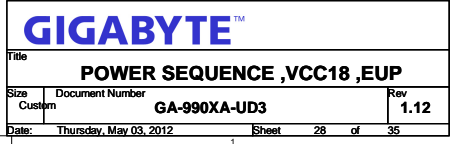
Title		
AUDIO JACK		
Size	Document Number	Rev
Custom	GA-990XA-UD3	1.12
Date:	Thursday, May 03, 2012	Sheet 24 of 35

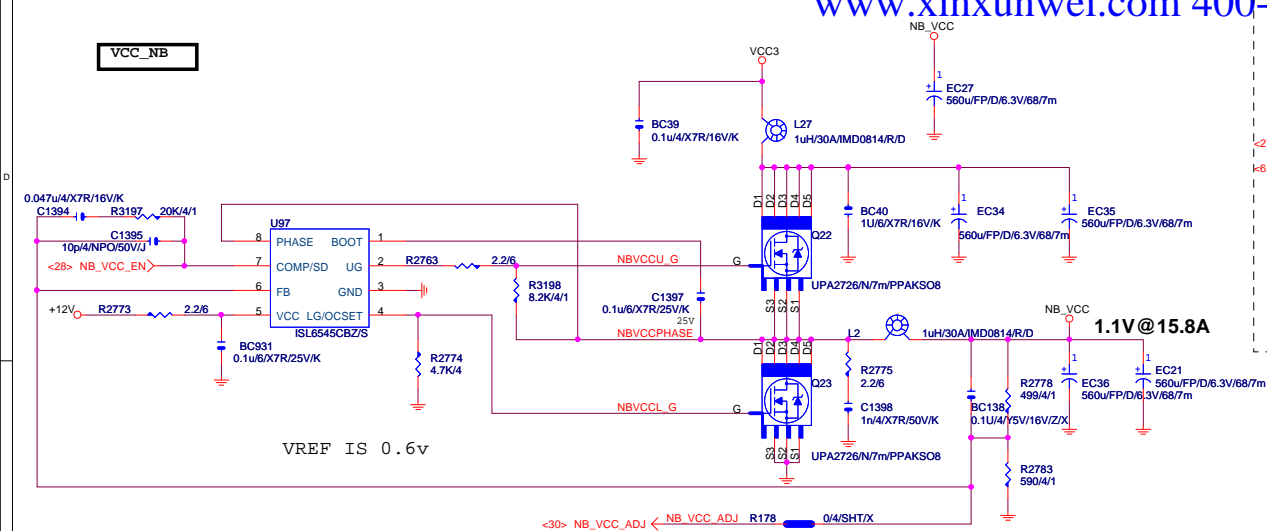
Hardware Monitor circuits









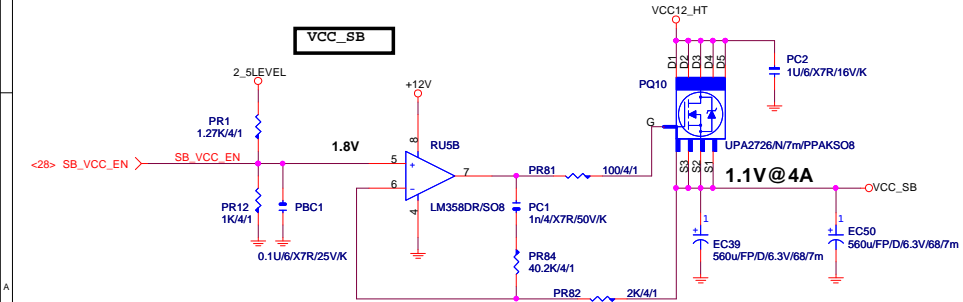
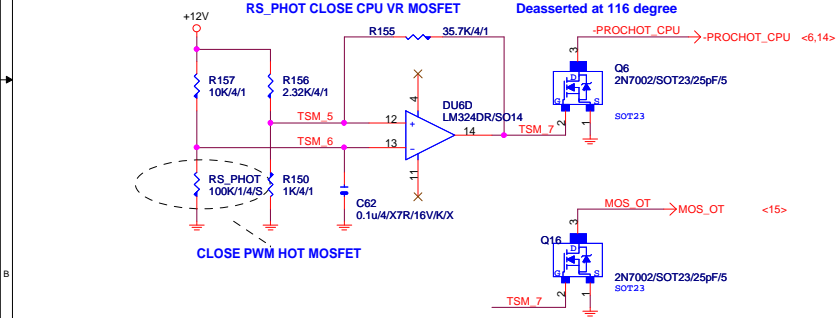
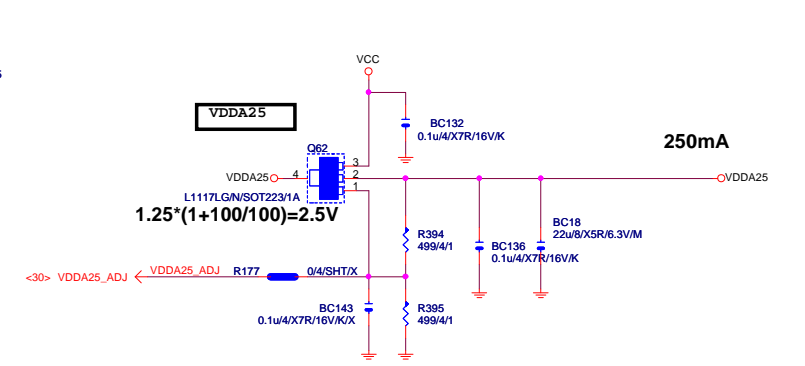
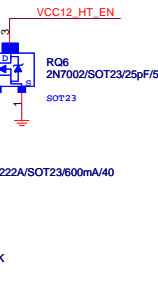
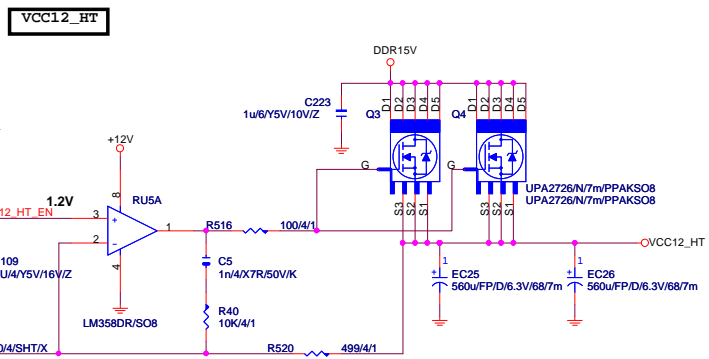
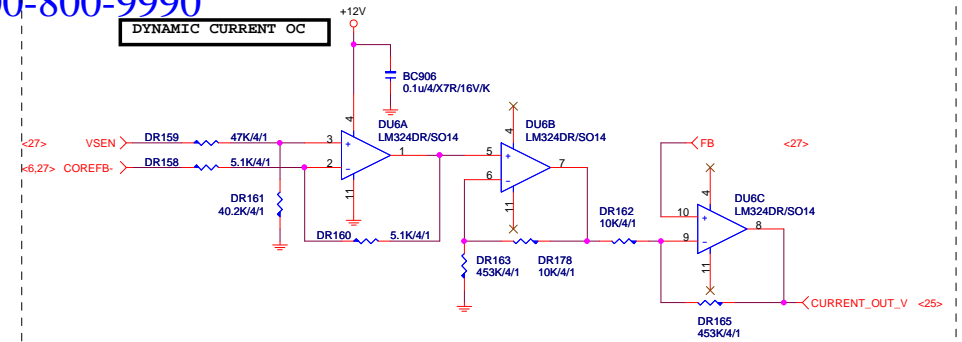


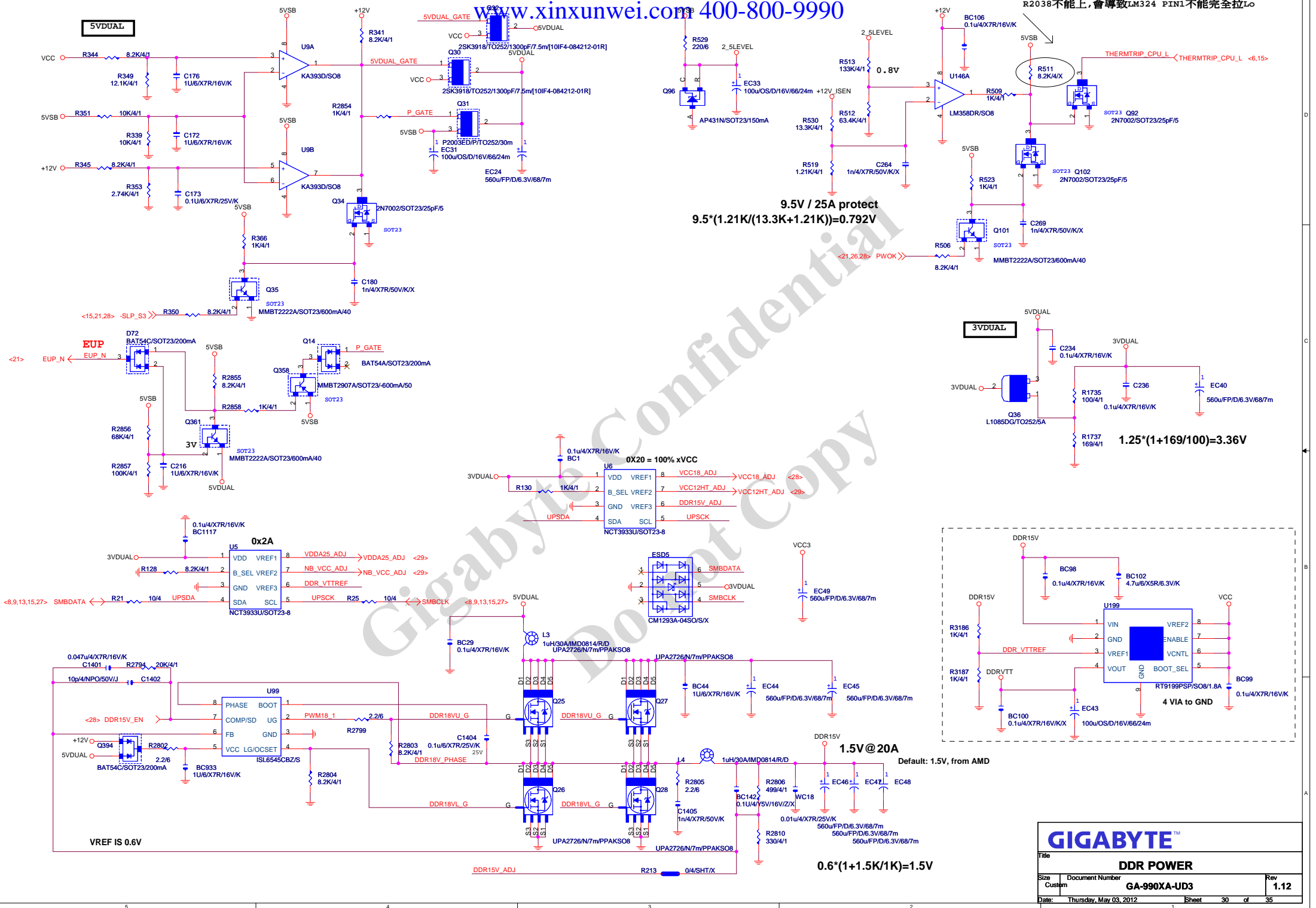
VREF IS 0.6v

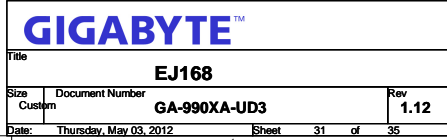
<30> NB_VCC_ADJ ← NB_VCC_ADJ R178 0/4/SHT/X

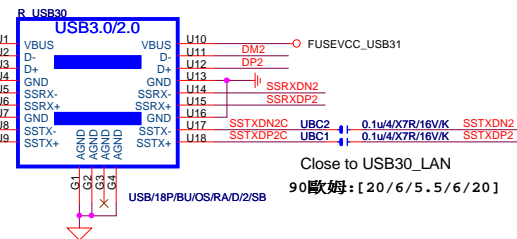
Default change to 1.15V

Patch AMD Validation VDDA25 & VCC12_HT power sequence

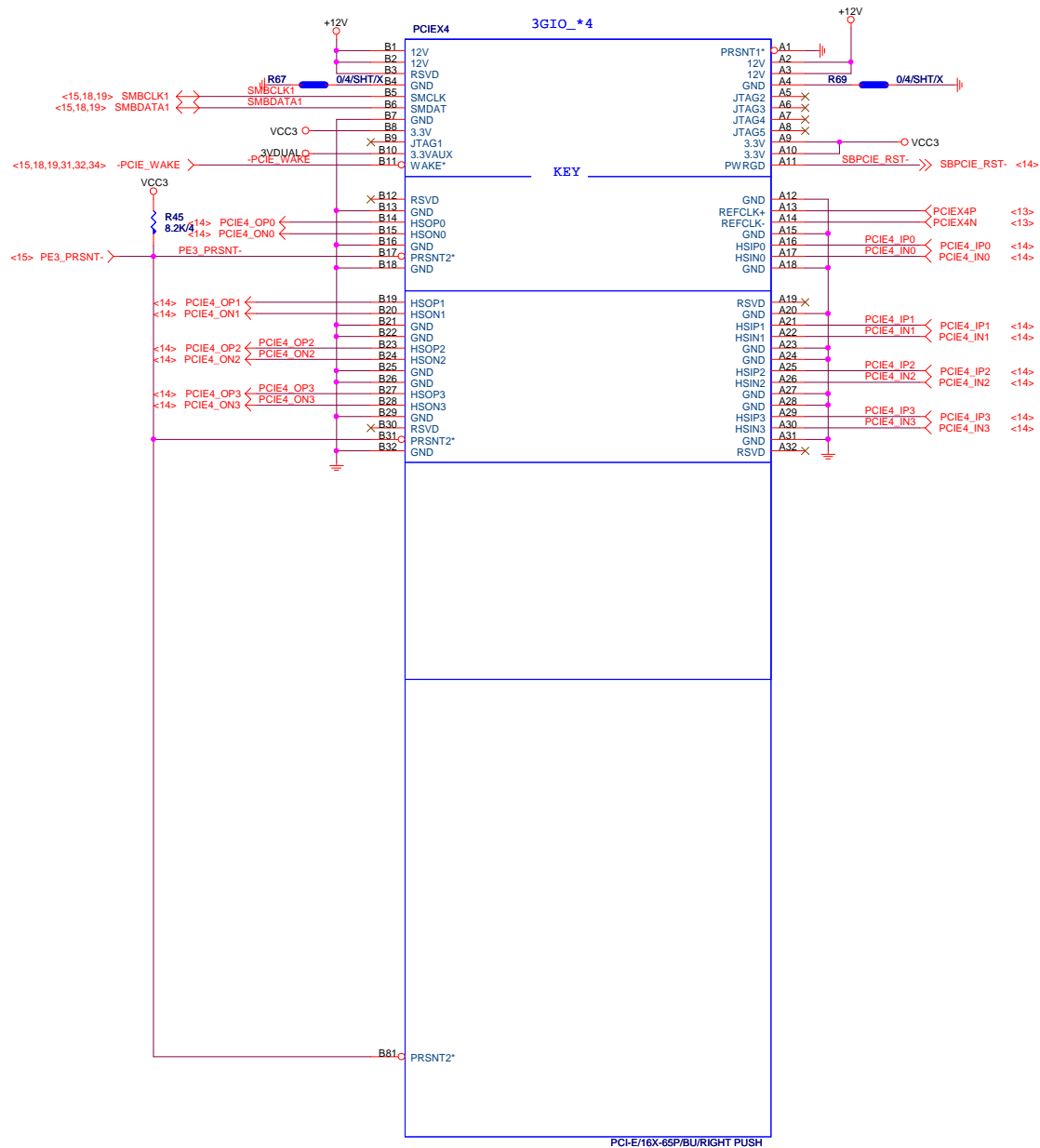


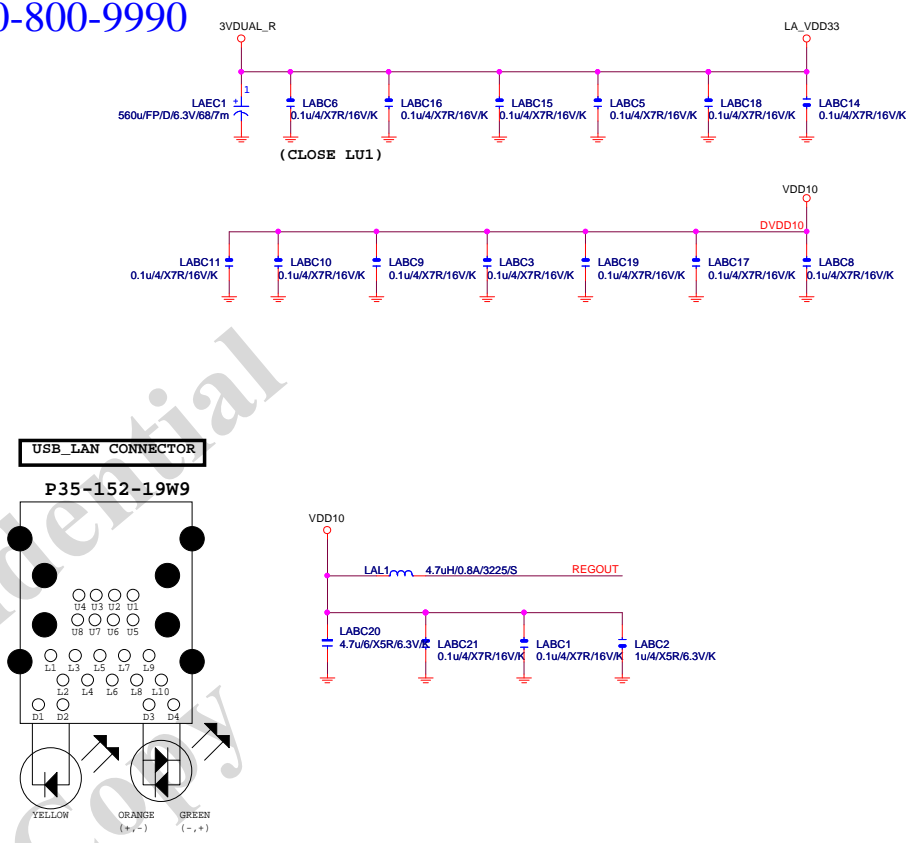






Close to USB30_LAN
90歐姆:[20/6/5.5/6/20

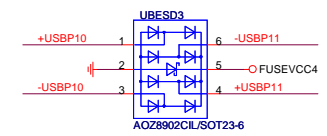


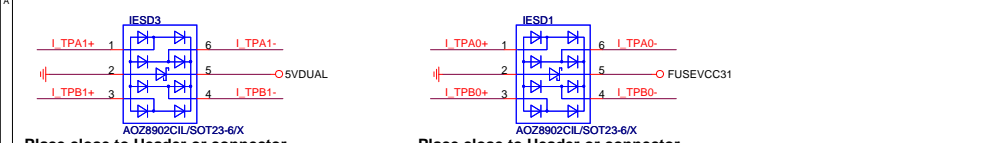
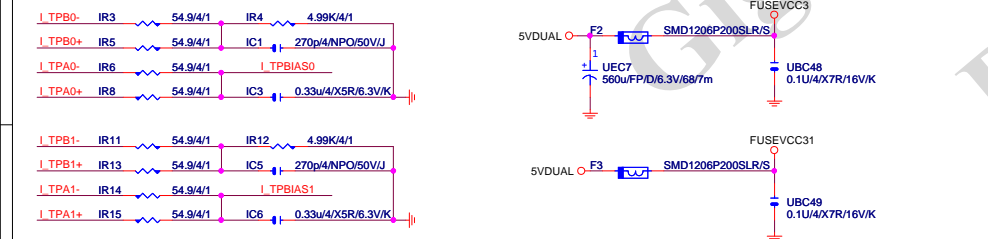
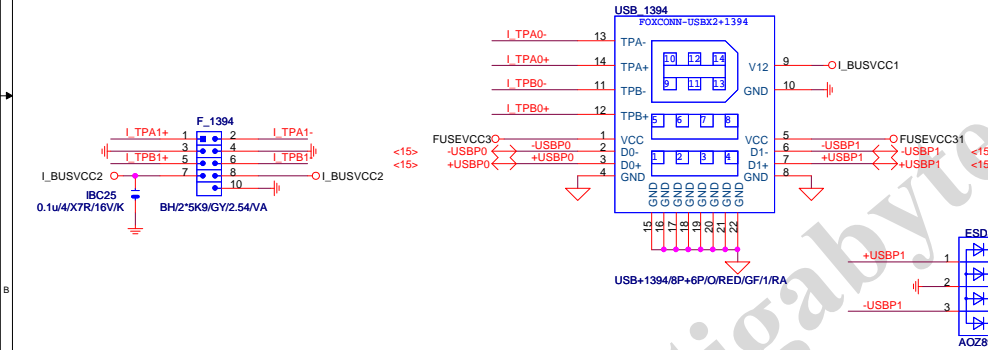
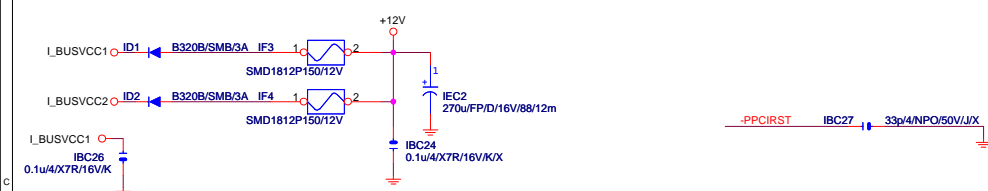
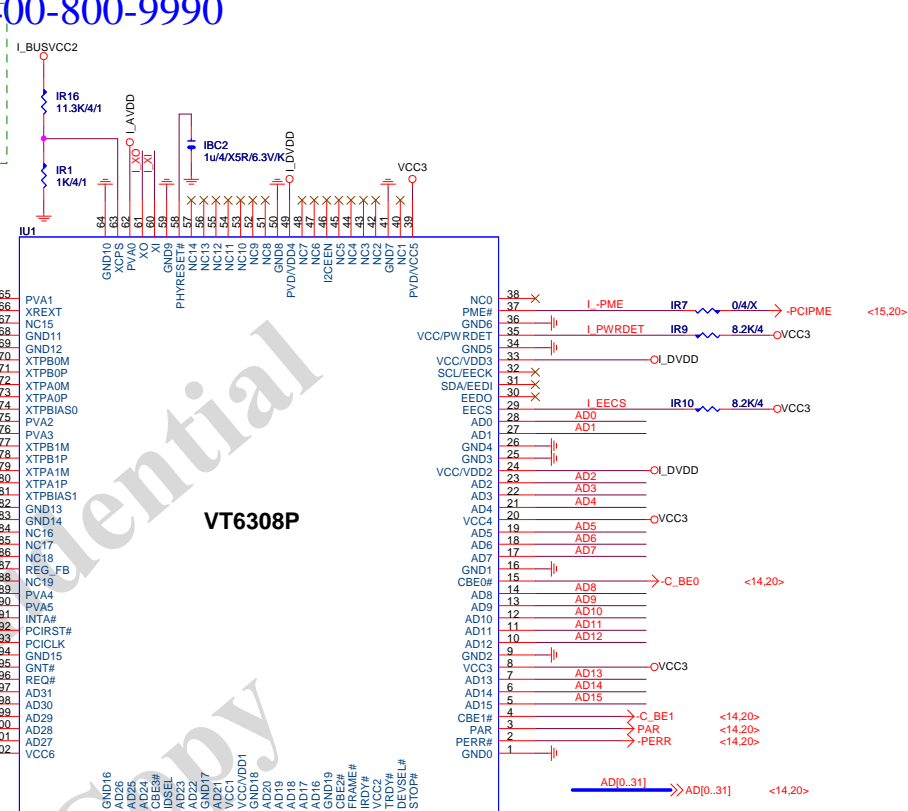
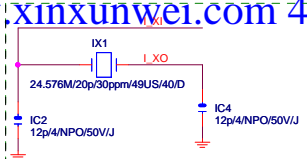
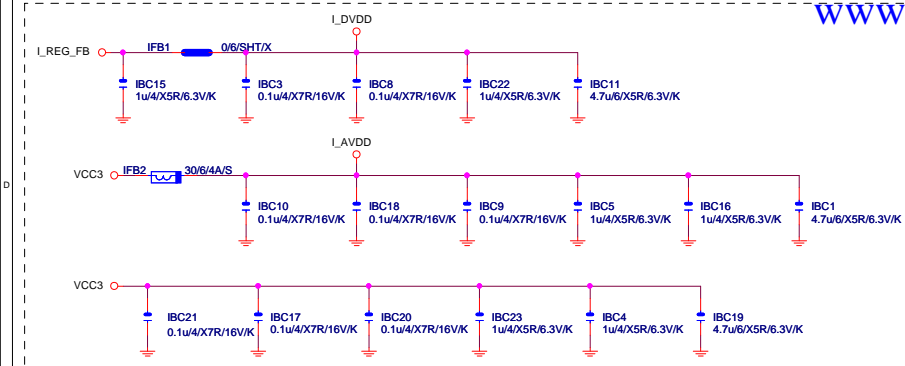


RTL8101E : L1+L10-->AVDD18+0.1u(BIOS DISABLE MDI-X FUNCTION)

1G : USB+LAN/1G/GO,Y/OS/RA/D/1

100M:USB+LAN/100/GO,Y/OS/RA/D/1





Place close to Header or connector

Place close to Header or connector